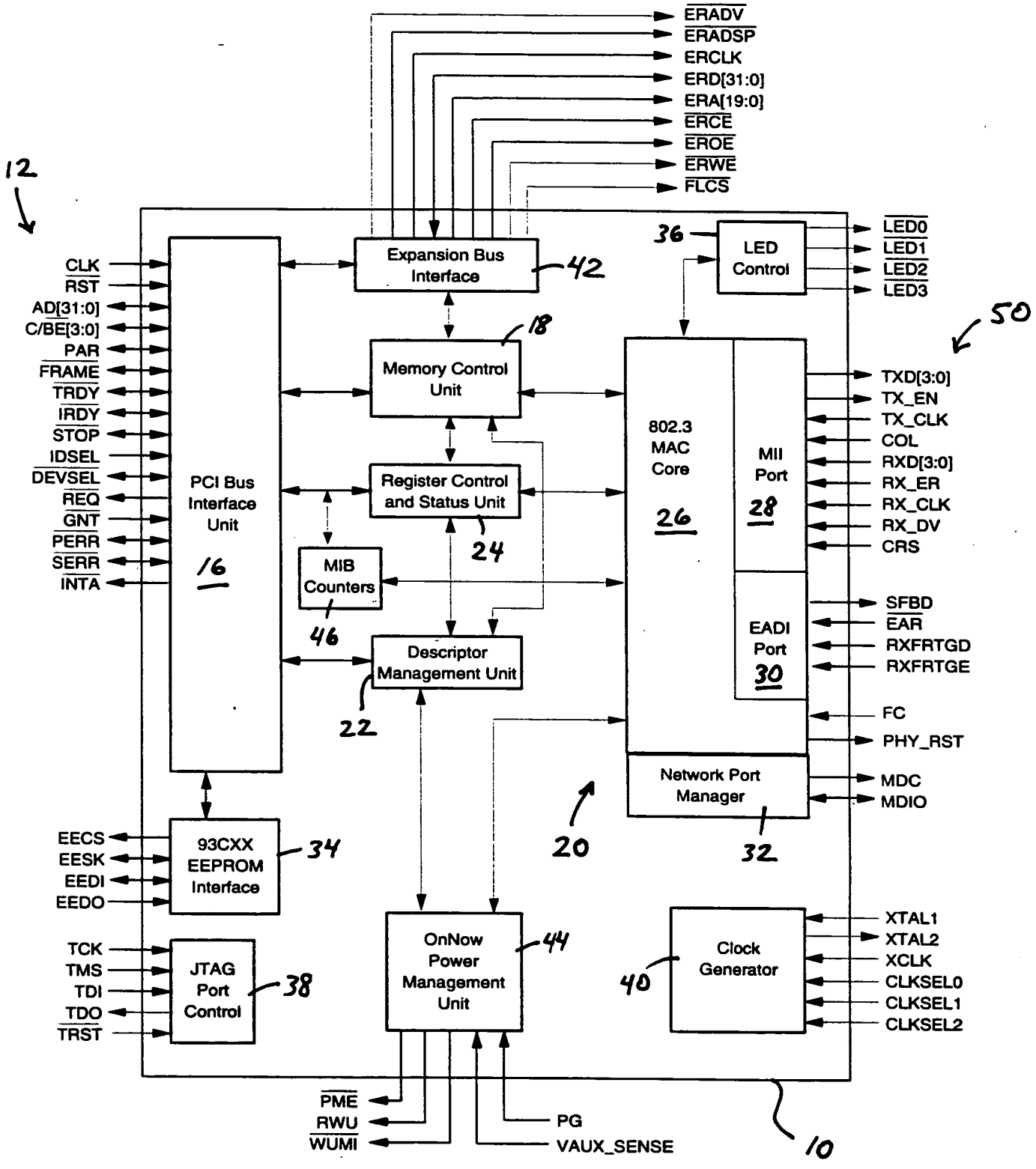

12
ERADV
ERADSP
ERCLK
ERD[31:0]
ERA[19:0]
ERCE
EROE
ERWE
FLCS
CLK
RST
AD[31:0]
C/BE[3:0]
PAR
FRAME
TRDY
IRDY
STOP
IDSEL
DEVSEL
REQ
GNT
PERR
SERR
INTA
PCI Bus Interface Unit
16
Expansion Bus Interface
42
Memory Control Unit
18
Register Control and Status Unit
24
MIB Counters
46
Descriptor Management Unit
22
36
LED Control
LED0
LED1
LED2
LED3
50
802.3 MAC Core
26
MII Port
28
EADI Port
30
TXD[3:0]
TX_EN
TX_CLK
COL
RXD[3:0]
RX_ER
RX_CLK
RX_DV
CRS
SFBD
EAR
RXFRTGD
RXFRTGE
FC
PHY_RST
Network Port Manager
32
MDC
MDIO
20
EECS
EESK
EEDI
EEDO
93CXX EEPROM Interface
34
TCK
TMS
TDI
TDO
TRST
JTAG Port Control
38
OnNow Power Management Unit
44
Clock Generator
40
XTAL1
XTAL2
XCLK
CLKSEL0
CLKSEL1
CLKSEL2
PME
RWU
WUMI
PG
VAUX_SENSE
10

Figure 1

00h TTO" 4262864

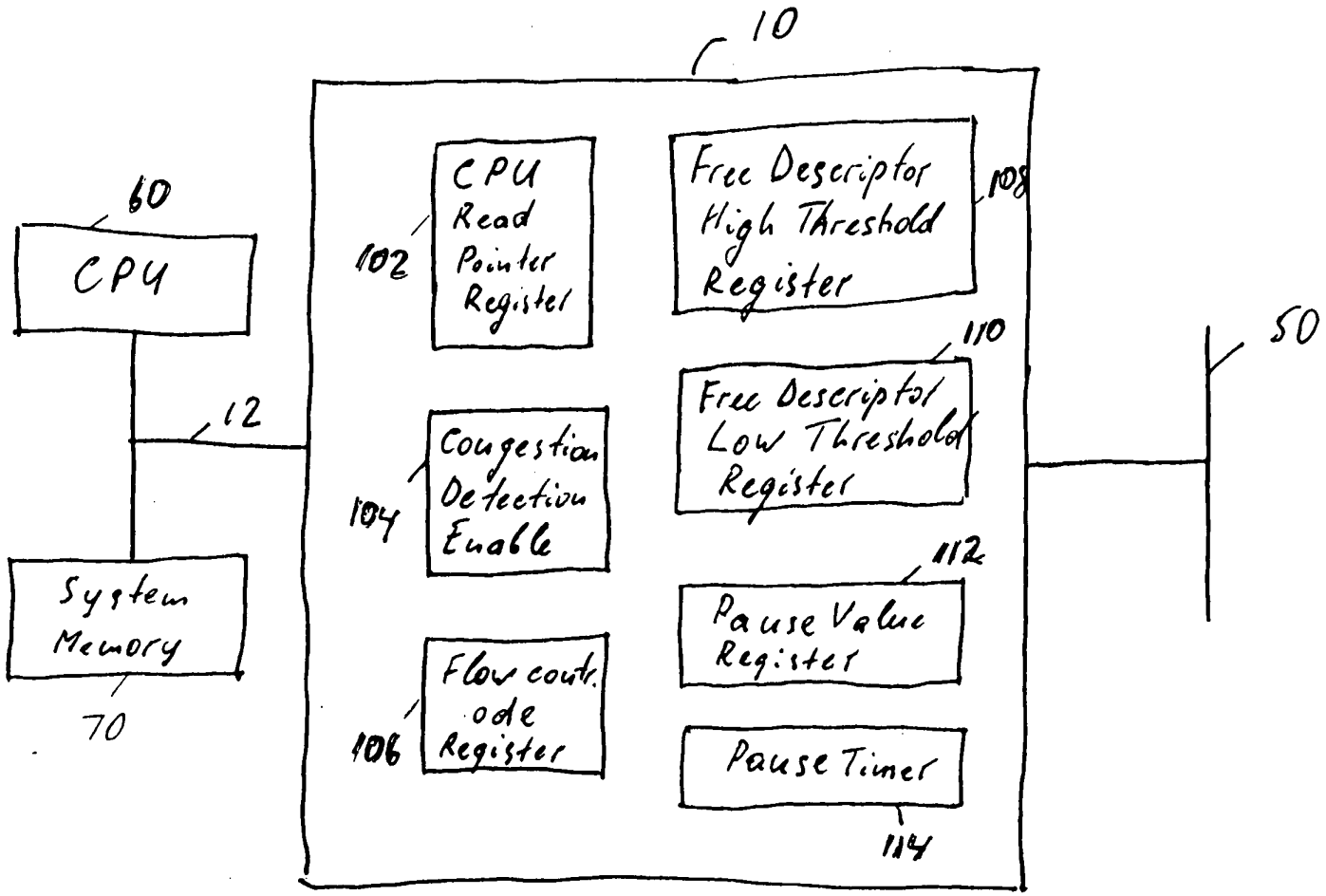
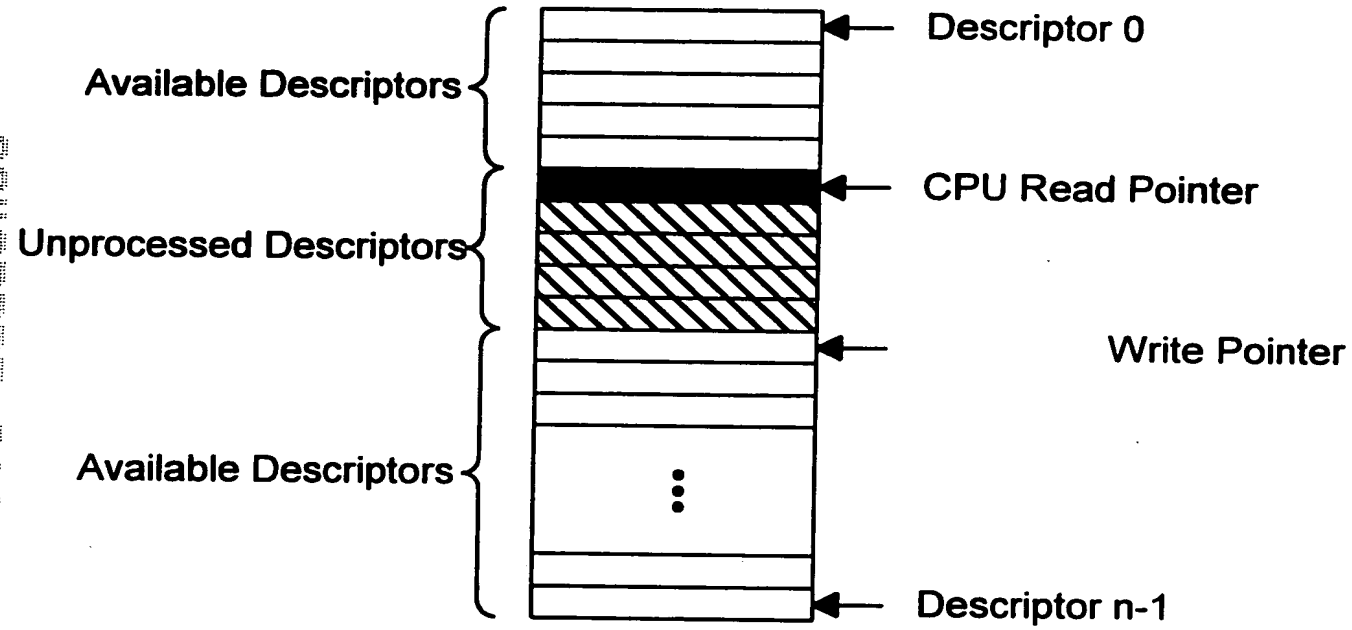



Figure 2

FIGURE 3


Descriptor 0
Available Descriptors
CPU Read Pointer
Unprocessed Descriptors
Write Pointer
Available Descriptors
Descriptor n-1